

Fig. 1

DETERMINATION CIRCUIT

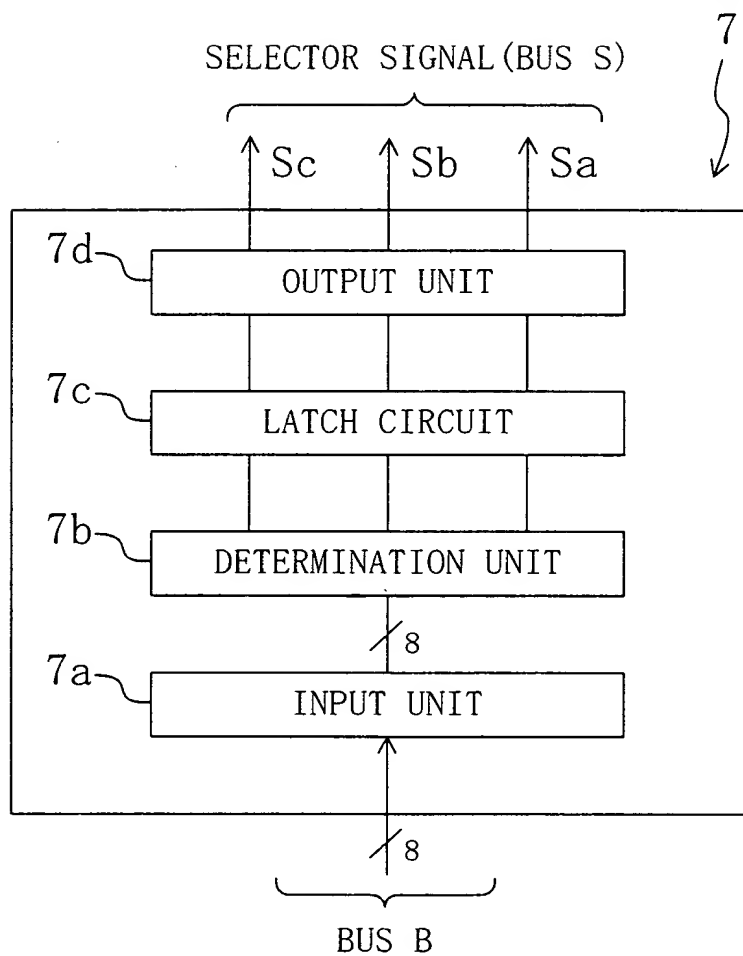


Fig. 3(a)

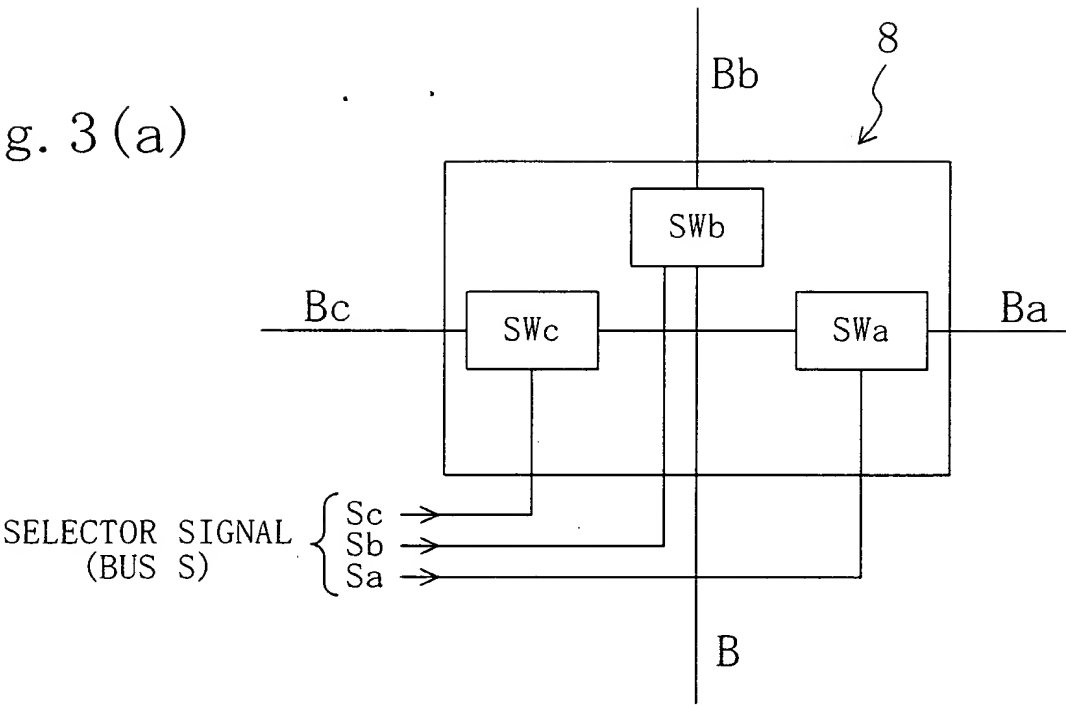


Fig. 3(b)

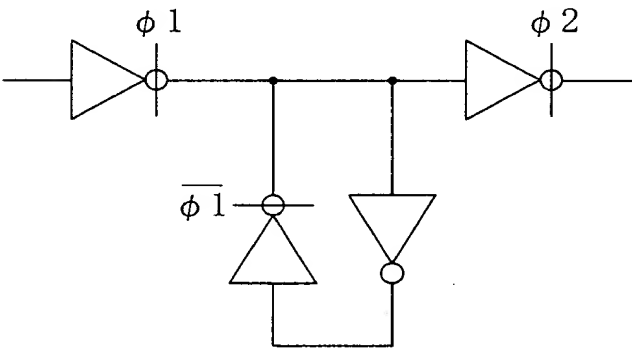
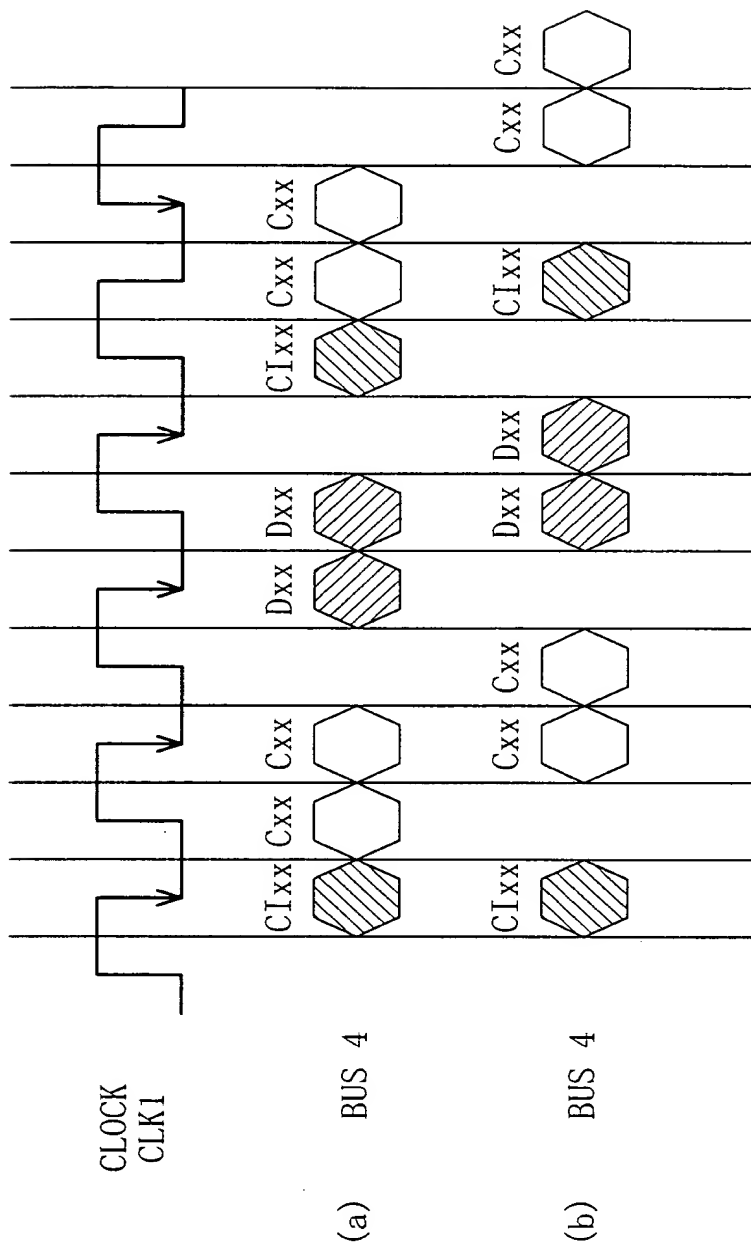


Fig. 3(c)

COMMAND SIGNAL C _{Ixx}		INFORMATION (DETERMINATION RESULTS)
SECOND BIT A	THIRD BIT B	
0	0	NO SELECTION
0	1	SLAVE a
1	0	SLAVE b
1	1	SLAVE c

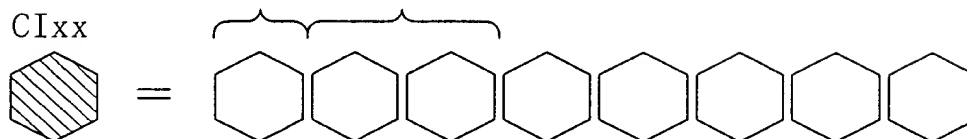
Fig. 4



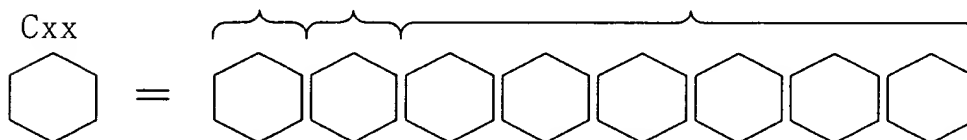
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Fig. 5

COMMAND	DETERMINATION
DESTINATION	INFORMATION OF
DETERMINATION	SELECTOR
INFORMATION	CIRCUIT 8



COMMAND	READ OR WRITE	ADDRESS
DESTINATION	DETERMINATION	
DETERMINATION	INFORMATION	
INFORMATION		



002050" 5522960

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Fig. 6

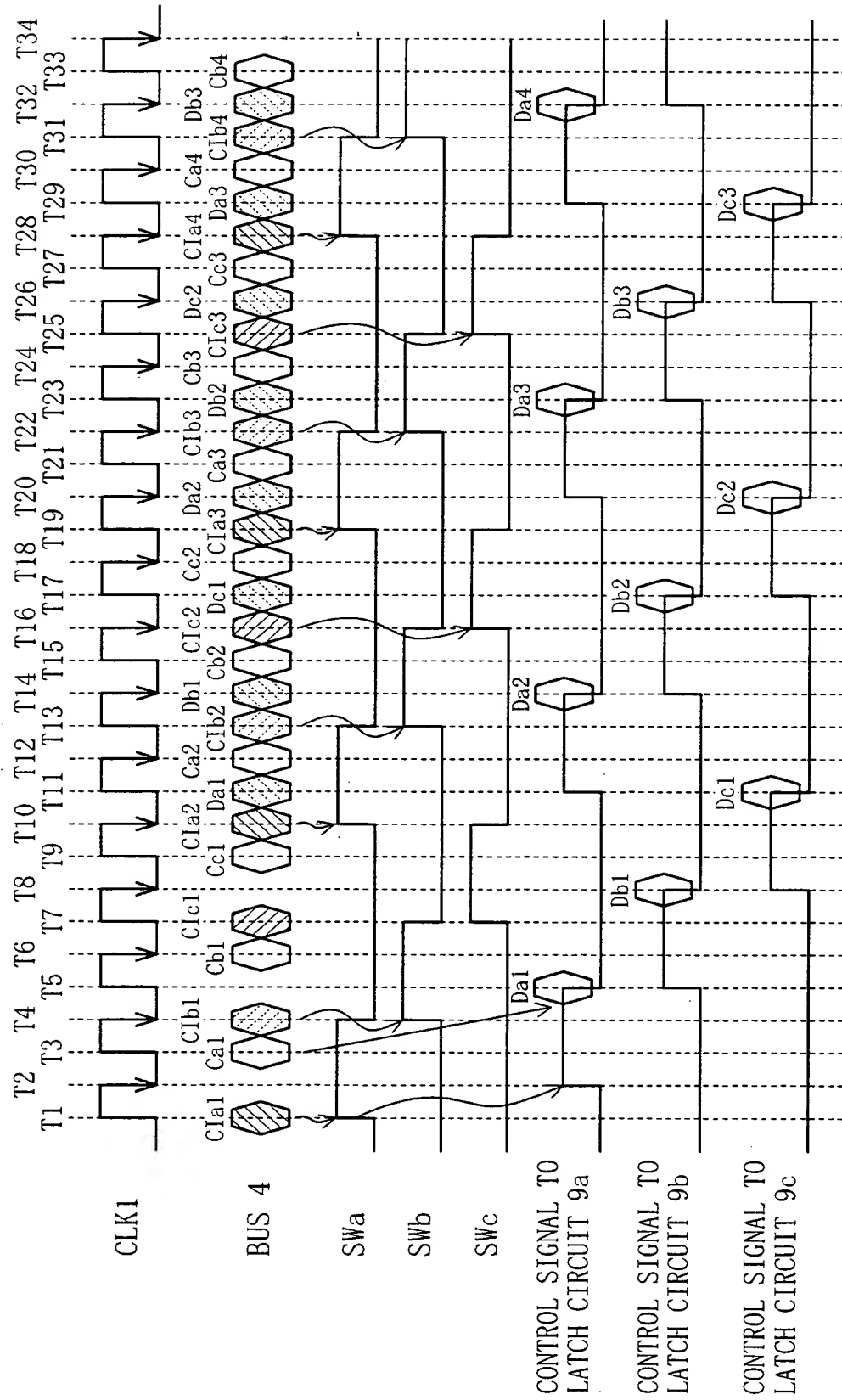
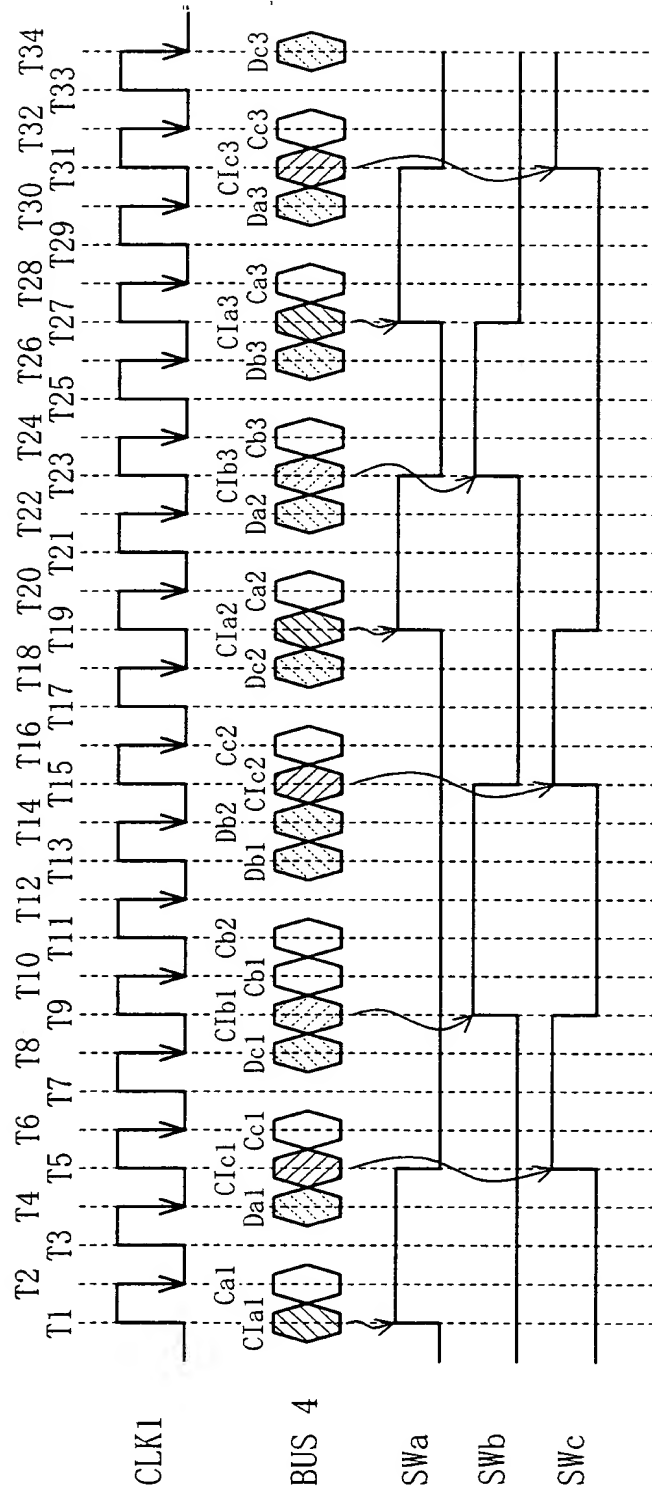


Fig. 7

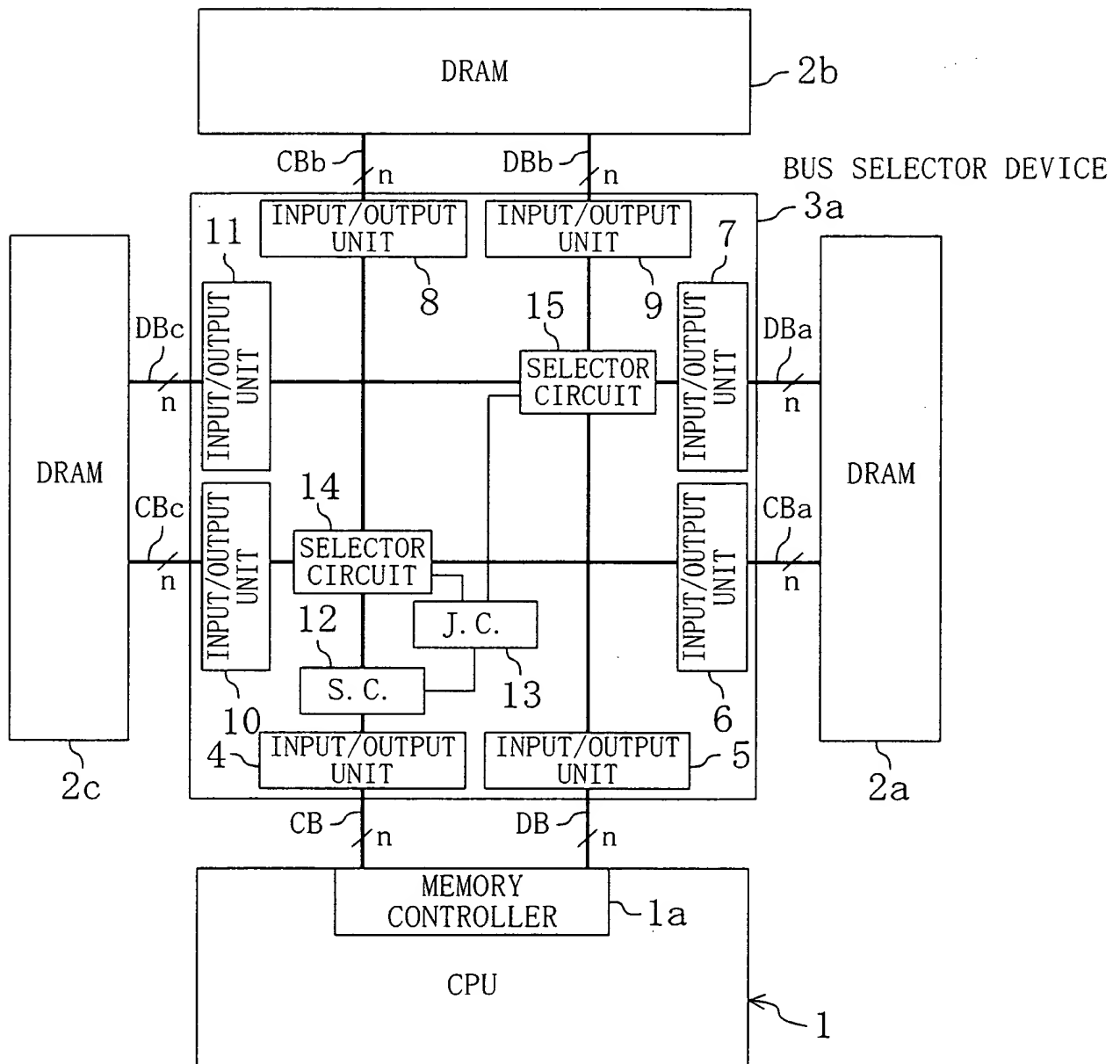


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Fig. 8

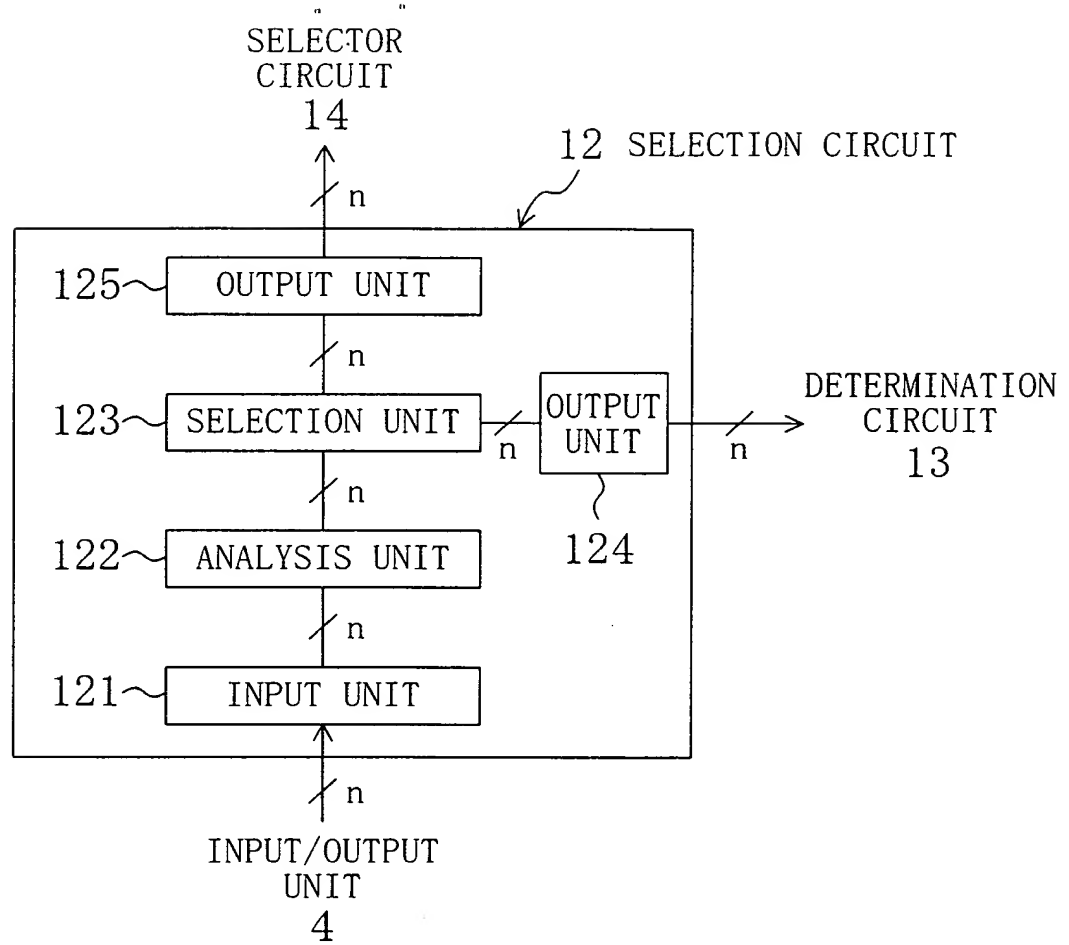
SEMICONDUCTOR INTEGRATED
CIRCUIT SYSTEM

110



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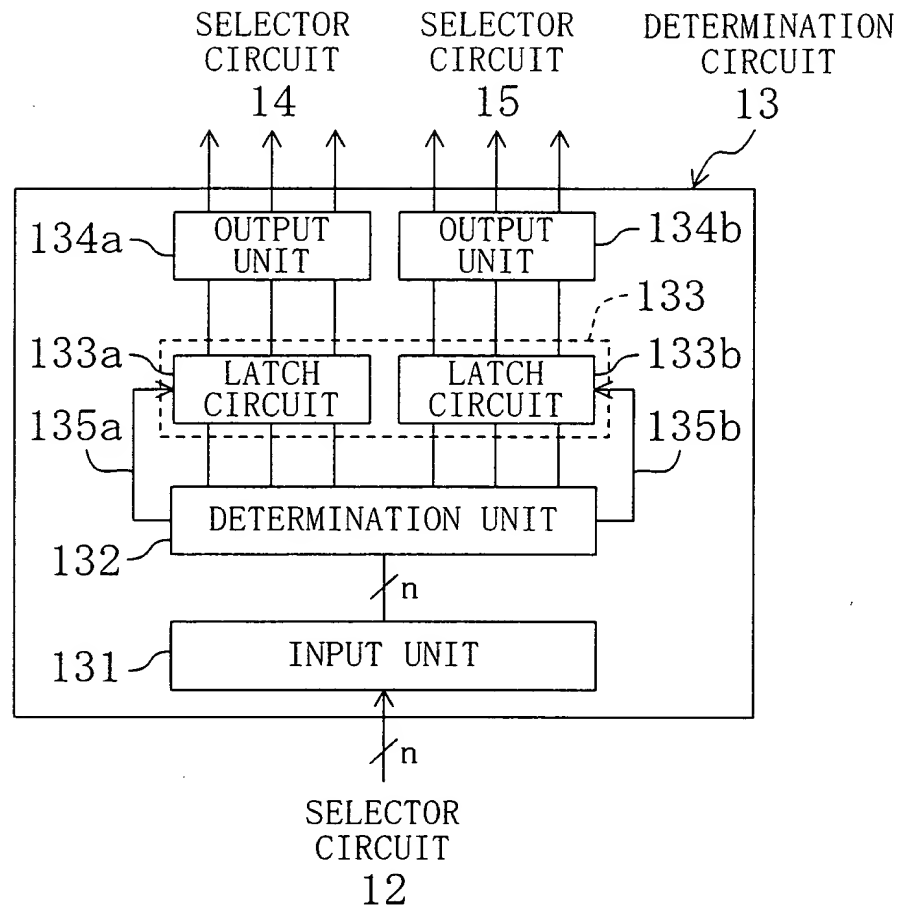
Fig. 9



00/060" 55922950

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Fig. 10



002050-55962960

Fig. 11(a)

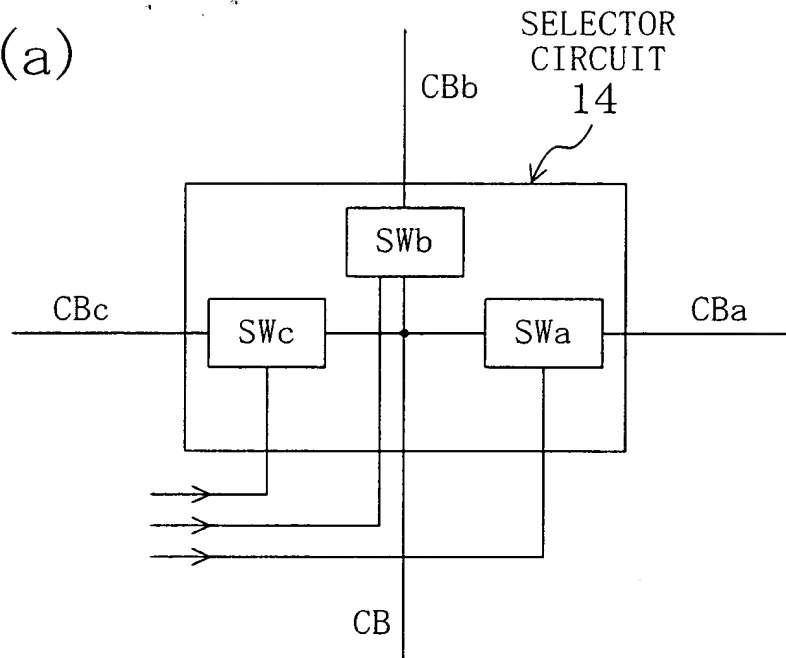


Fig. 11(b)

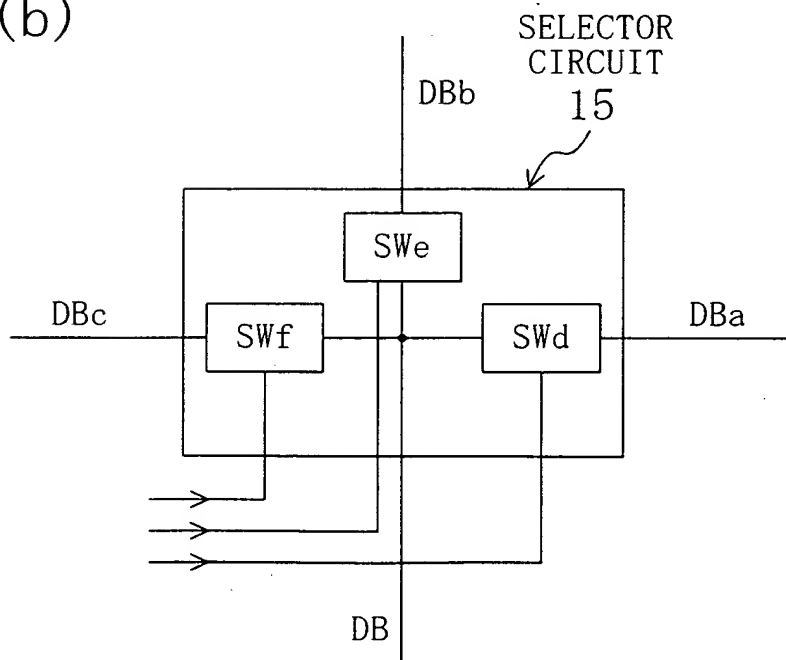
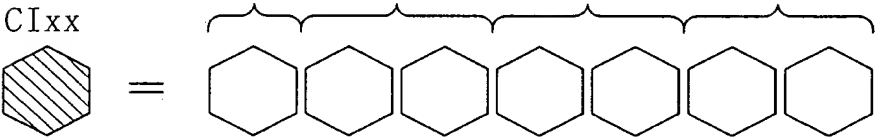


Fig. 12

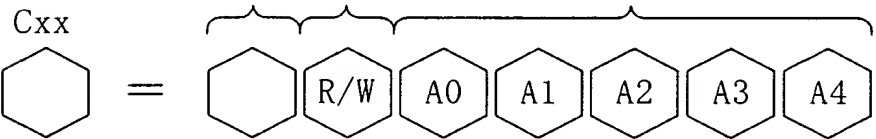
COMMAND	SELECTOR	SELECTOR	SELECTOR
DESTINATION	CIRCUITS 14, 15	CIRCUIT 14	CIRCUIT 15
DETERMINATION	DETERMINATION	CONTROL	CONTROL
INFORMATION	INFORMATION	INFORMATION	INFORMATION

BUS SELECTION
CONTROL
COMMAND



COMMAND	READ OR WRITE	ADDRESS
DESTINATION	DETERMINATION	INFORMATION
DETERMINATION	INFORMATION	
INFORMATION		

SLAVE CONTROL
COMMAND



COMMAND	READ OR WRITE	DATA
DESTINATION	DETERMINATION	INFORMATION
DETERMINATION	INFORMATION	
INFORMATION		

DATA

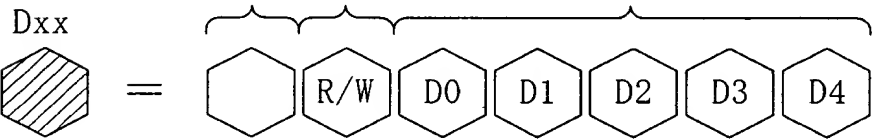


Fig. 13

INPUT	DETERMINATION	
A		
0		TO J. C. (13)
1		TO SELECTOR CIRCUIT 14

INPUT		DETERMINATION
B	C	
0	0	—
0	1	TO SELECTOR CIRCUIT 14
1	0	TO SELECTOR CIRCUIT 15
1	1	14&15

INPUT		DETERMINATION IN SELECTOR CIRCUIT 14
D	E	
0	0	—
0	1	SWa
1	0	SWb
1	1	SWc

INPUT		DETERMINATION IN SELECTOR CIRCUIT 15
F	G	
0	0	—
0	1	SWd
1	0	SWe
1	1	SWf

002050" 55932960

Fig. 14

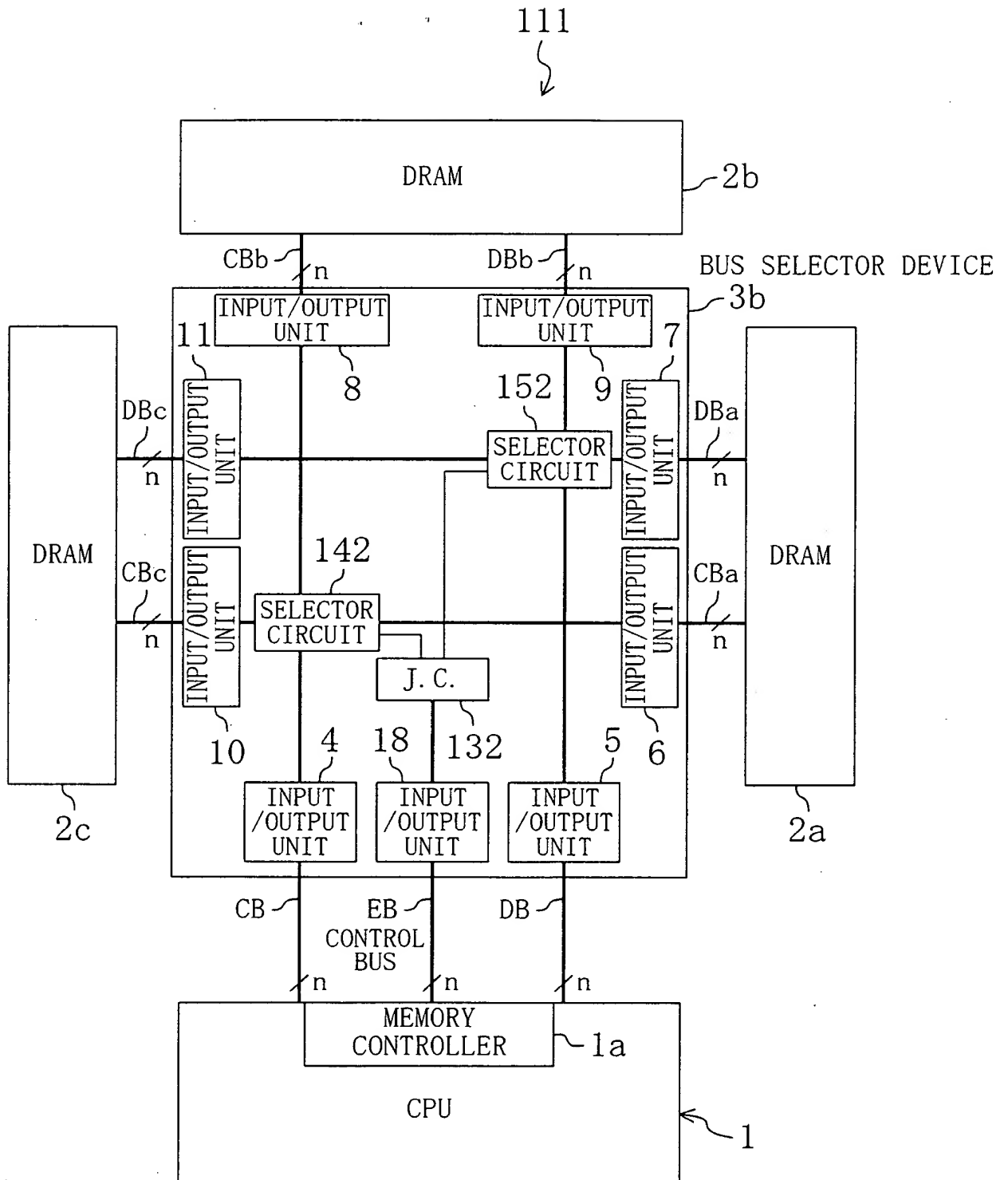
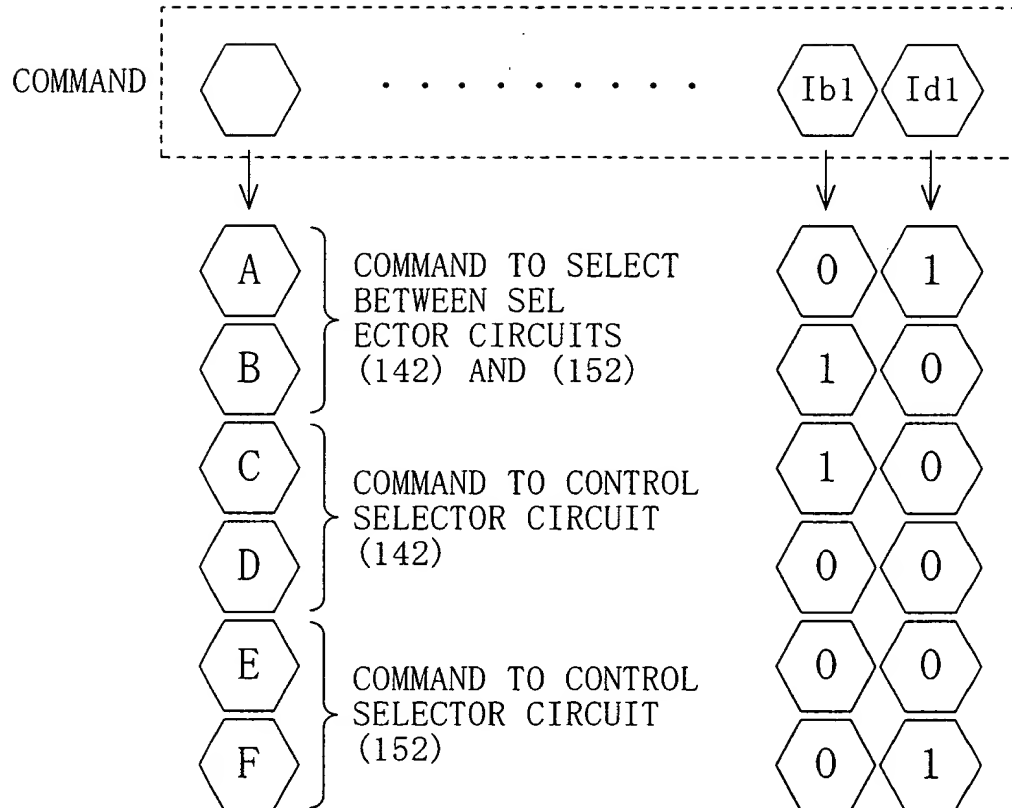


Fig. 15



002060" 559E2960

Fig. 16

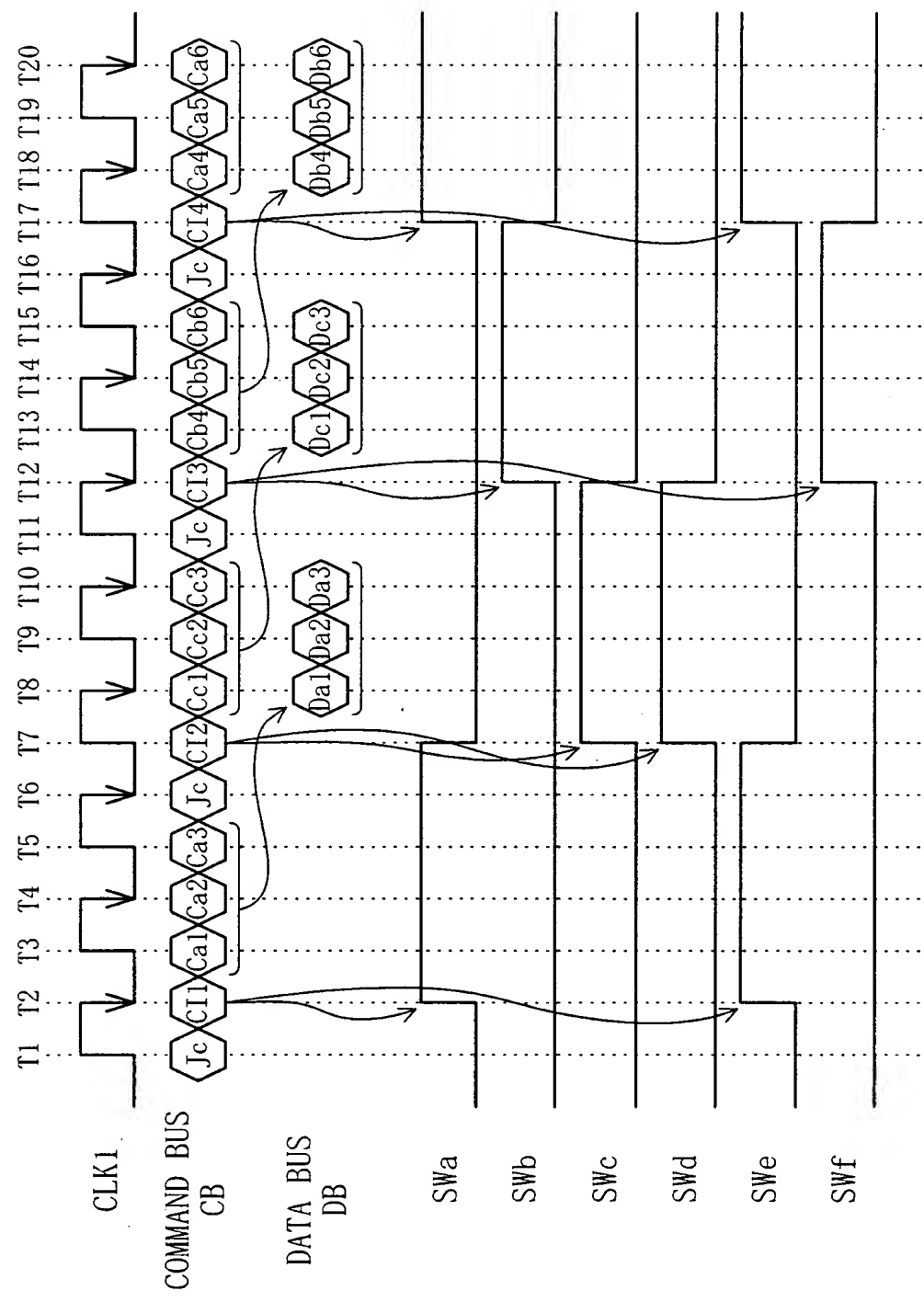


Fig. 17

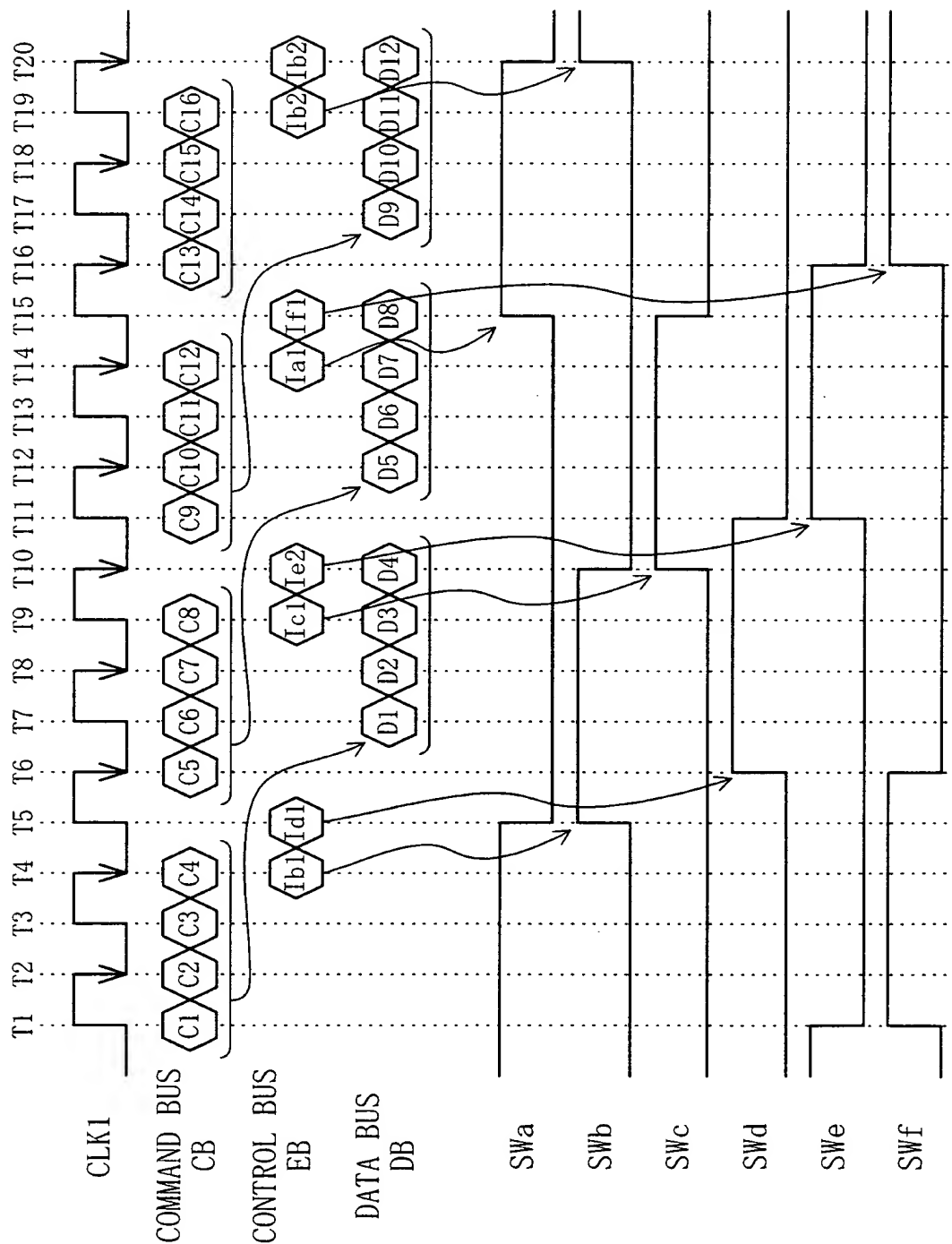
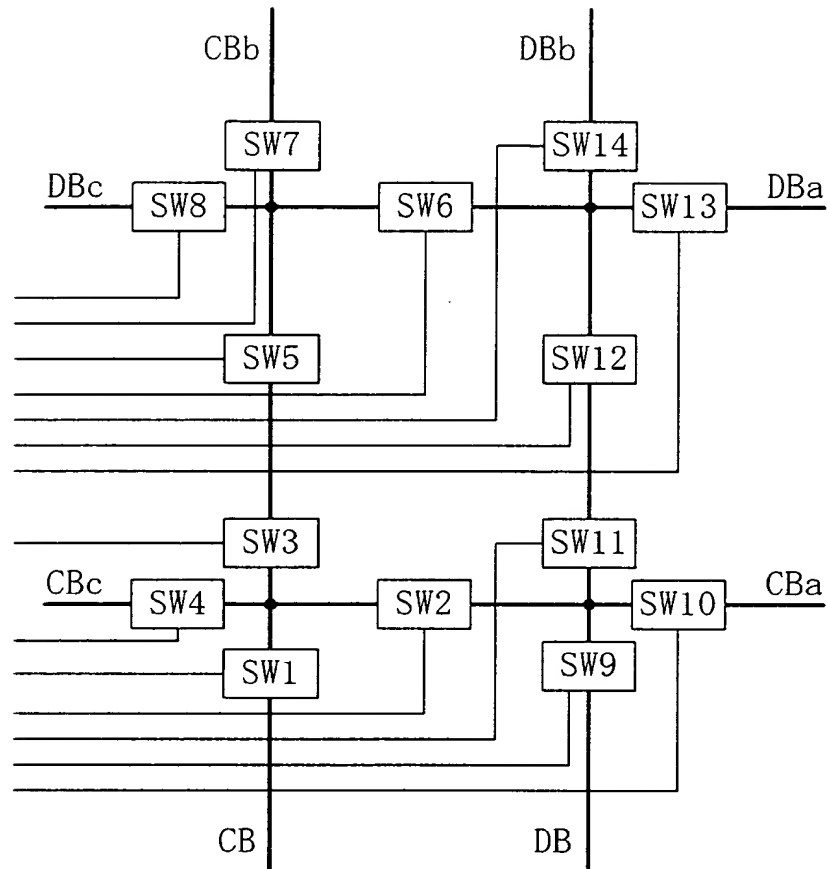


Fig. 18



002060" 599E2360

Fig. 19

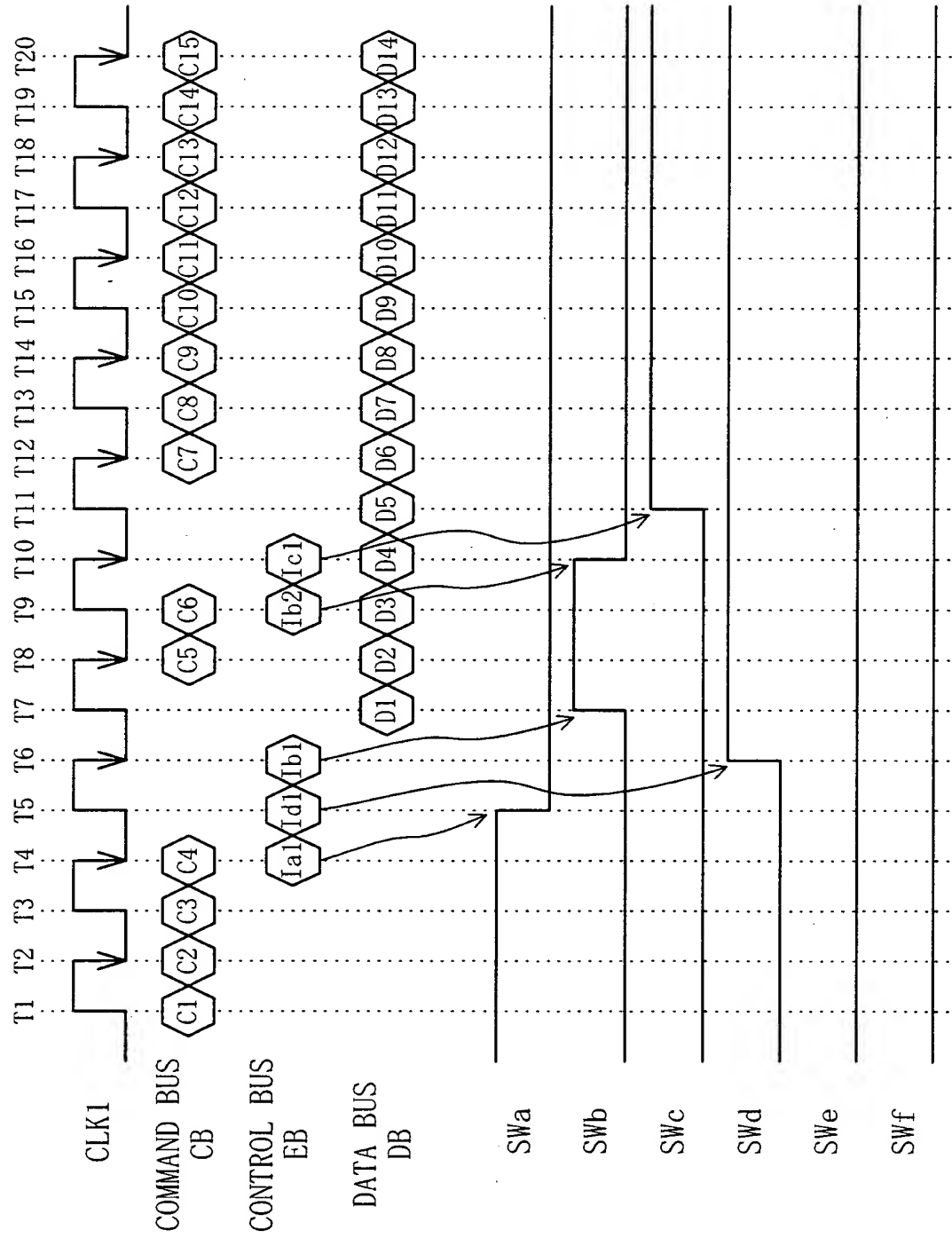


Fig. 20

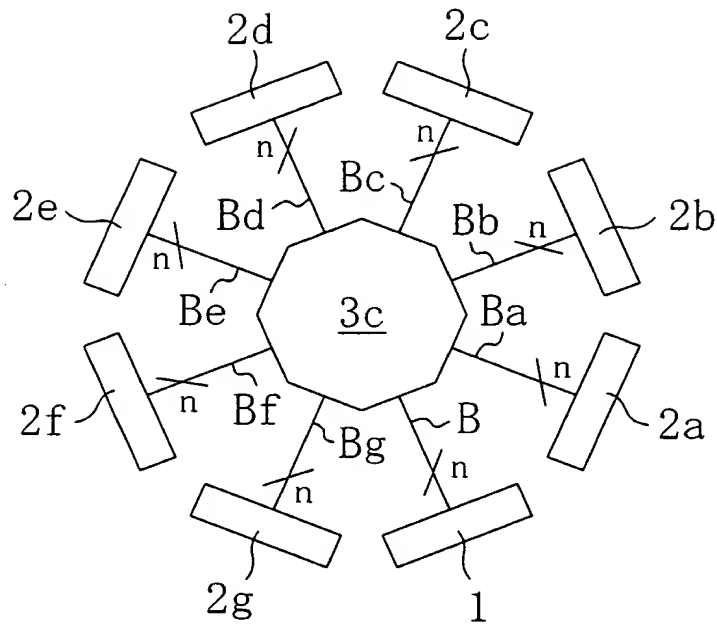


Fig. 21(a)

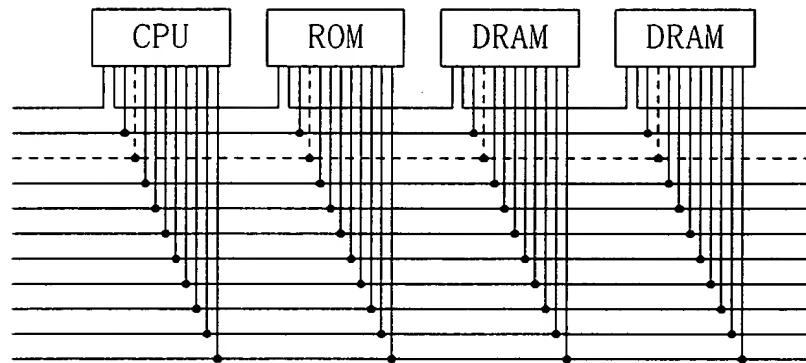


Fig. 21(b)

